

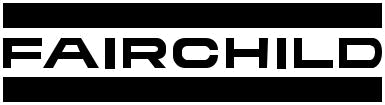
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**Nota de Aplicação 42047**

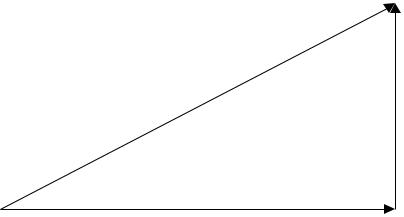
**Noções básicas de correção de fator de potência (PFC)**

**O que é o fator de potência?**

O fator de potência (PF) é definido como a relação entre a potência real (P) e a potência aparente (S) ou o cosseno (para onda senoidal pura para corrente e tensão) que representa o ângulo de fase entre a corrente e a tensão veja a figura 1). O fator de potência pode variar entre 0 e 1, e pode ser indutivo (em atraso, apontando para cima) ou capacitivo (em avanço, apontando para baixo). Para reduzir um atraso indutivo, os capacitores são adicionados até que PF seja igual a 1. Quando as formas de onda de corrente e tensão estão em fase, o fator de potência é 1 (cos (0 °) = 1). O propósito de tornar o fator de potência igual a um é fazer com que o circuito pareça puramente resistivo (potência aparente igual à potência real).

Potência real (watts) produz trabalho real; este é o componente de transferência de energia (exemplo rpm eletricidade motor). A energia reativa é a potência necessária para produzir os campos magnéticos (potência perdida) para permitir que o trabalho real seja realizado, onde a energia aparente é considerada a potência total que a empresa fornece, conforme mostrado na Figura 1. Essa potência total é a energia fornecida através da rede elétrica para produzir a quantidade necessária de energia real.

“Potência Total”



Poder aparente

(S) = Volt Amperes = I2Z

Potência Reativa

(Q) = vars = (XL – XC) | 2

θ

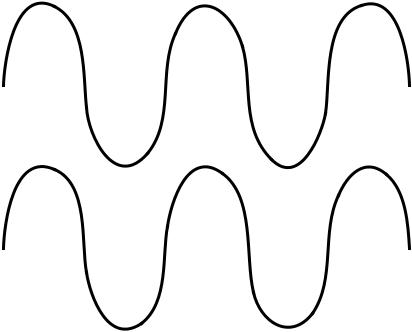
Potência Real

(P) = Watts = (I2R)

Quando o fator de potência não é igual a 1, a forma de onda atual não segue a forma de onda da tensão. Isso resulta não apenas em perdas de energia, mas também pode causar harmônicos que percorrem a linha neutra e interrompem outros dispositivos conectados à linha. Quanto mais próximo o fator de potência for de 1, mais próximos os harmônicos de corrente serão de zero, já que toda a energia está contida na frequência fundamental.

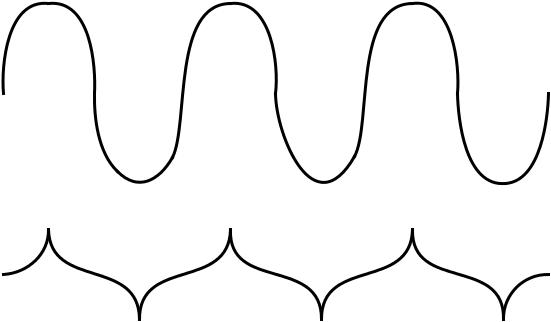
**Entendendo Regulamentos Recentes**

Em 2001, a União Europeia pôs em prática o EN61000-3-2 para estabelecer limites nas harmônicas da corrente de entrada (CA) até a 40ª harmônica. Antes da EN61000-3-2 entrar em vigor, foi aprovada uma emenda em outubro de 2000 que declarava que os únicos dispositivos necessários para passar os rigorosos limites de emissão da Classe D (Figura 2) são computadores pessoais, monitores de computador pessoal e receptores de televisão. Outros dispositivos só foram obrigados a passar os limites de emissão relaxados Classe A (Figura 3).



**13,5**

**Figure 1. Triângulo do fator de potência (atraso)**



A definição previamente estabelecida do fator de potência relacionado ao ângulo de fase é válida quando consideradas as formas de onda sinusoidais ideais para corrente e tensão; no entanto, a maioria das fontes de alimentação desenham uma corrente não senoidal. Quando a corrente não é sinusoidal e a tensão é sinusoidal, o fator de potência consiste em dois fatores: 1) o fator de deslocamento relacionado ao ângulo de fase e 2) o fator de distorção relacionado à forma de onda. A equação 1 representa a relação entre o deslocamento e o fator de distorção em relação ao fator de potência.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| *PF* = | *Irms*(1) | cos*θ* = *Kd* ⋅ *Kθ* | (1) |  |
|  |  |
|  | *Irms* | |  |  |

Irms (1) é o componente fundamental da corrente e Irms é o valor atual do RMS. Portanto, a finalidade do circuito de correção do fator de potência é minimizar a distorção da corrente de entrada e fazer a corrente em fase com a tensão.

**Figura 3: Isto é o que é chamado de entrada quasi-PFC,**

**Alcançar um pF em torno de 0,9 (classe A)**

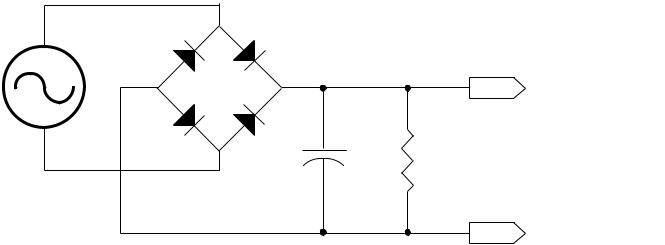
**Causas de Ineficiências**

Um problema com as fontes de alimentação comutadas (SMPS) é que elas não usam qualquer forma de correção do fator de potência e que o capacitor de entrada CIN (mostrado na Figura 4) só carregará quando VIN estiver próximo a VPEAK ou quando VIN for maior

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que a tensão do capacitor VCIN. Se o CIN for projetado usando a frequência de tensão de entrada, a corrente ficará muito mais próxima da forma de onda de entrada (dependente do nível de som); no entanto, qualquer pequena interrupção na linha principal fará com que todo o sistema reaja negativamente. Ao dizer que, ao projetar um SMPS, o tempo de espera para o CIN é projetado para ser maior que a frequência do VIN, de modo que se houver uma falha no VIN e alguns ciclos forem perdidos, o CIN terá energia suficiente armazenado para continuar a alimentar a sua



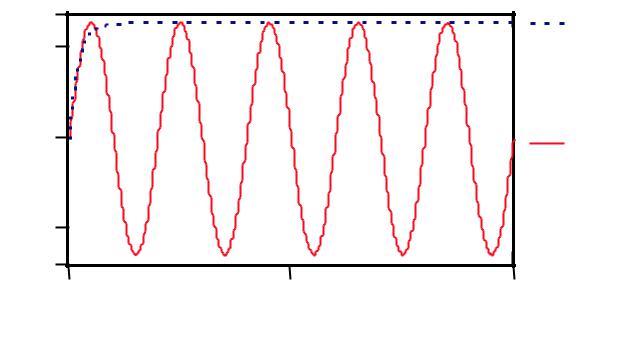
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | D1 |  |  |
| V1 | – | + | Vo (to PWM) |  |
|  |  |
|  |  |  |  |

Cin R1

RTN

**Figura 4. Entrada do SMPS sem o PFC**

Figure 5 represents a theoretical result of VCIN(t) (shown in the circuit in Figure 4) with a very light load, and hence, very little discharge of CIN. As the load impedance increases, there will be more droop from VCIN(t) between subsequent peaks, but only a small percentage with respect to the overall VIN (e.g. with the input being 120V, maybe a 3-5 volt droop. As previously stated, CIN will only charge when VIN is greater than its stored voltage, meaning that a non-PFC cir-cuit will only charge CIN a small percentage of the overall cycle time.



|  |  |  |  |
| --- | --- | --- | --- |
| 130 |  | Vc(t) |  |
| 100 |  |  |
|  |  |  |
| 0 |  | Vin(t) |  |
| -100 |  |  |  |
| -130 |  |  |  |
| 0 | 50 | 100 |  |

Time (s)

**Figure 5. VIN with Charging CIN**

After 90 degrees (Figure 6), the half cycle from the bridge

drops below the capacitor voltage (CIN); which back biases

the bridge, inhibiting current flow into the capacitor (via

VIN). Notice how big the input current spike of the inductor

is. All the circuitry in the supply chain (the wall wiring, the

diodes in the bridge, circuit breakers, etc) must be capable of

carrying this huge peak current. During these short periods

the CIN must be fully charged, therefore large pulses of cur-

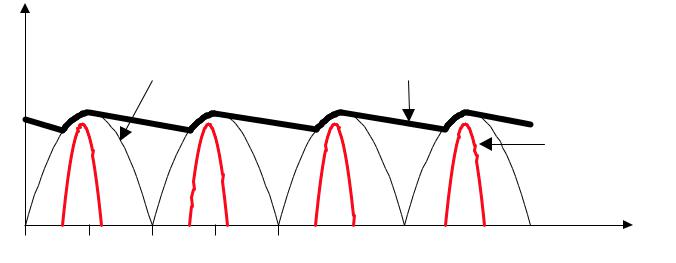
rent for a short duration are drawn from VIN. There is a way

to average this spike out so it can use the rest of the cycle to

accumulate energy, in essence smoothing out the huge peak

current, by using power factor correction.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| V |  |  |  |  |  |  |
|  | Input Voltage | | | Charging Bulk Input |  |  |
|  | (Full Rectified) | | | Capacitor Voltage (Vcin) |  |  |
|  |  |  |  |  | Input Current |  |
| 0 | 90 | 180 | 270 | 360 | Deg |  |
|  |  |



**Figure 6. Voltage and Current Waveforms in a**

**Simple Rectifier Circuit**

In order to follow VIN more closely and not have these high amplitude current pulses, CIN must charge over the entire cycle rather than just a small portion of it. Today’s non-linear loads make it impossible to know when a large surge of cur-rent will be required, so keeping the inrush to the capacitor constant over the entire cycle is beneficial and allows a much smaller CIN to be used. This method is called power factor correction.

**Boost Converters the Heart of Power Factor Correction**

Boost converter topology is used to accomplish this active power-factor correction in many discontinuous/continuous modes. The boost converter is used because it is easy to implement and works well. The simple circuit in Figure 7 is a short refresher of how inductors can produce very high voltages. Initially, the inductor is assumed to be uncharged, so the voltage VO is equal to VIN**.** When the switch closes, the current (IL) gradually increases through it linearly since:

1

*I L* = *L* ∫*VL dt***.**

Voltage (VL) across it increases exponentially until it stabi-lizes at VIN. Notice the polarity of the voltage across the inductor, as it is defined by the current direction (inflow side is positive). When the switch opens causing the current to change from Imax to zero (which is a decrease, or a negative slope). Looking at it mathematically:

*VL* = *L di* ≈ *L* ∆*i* ,

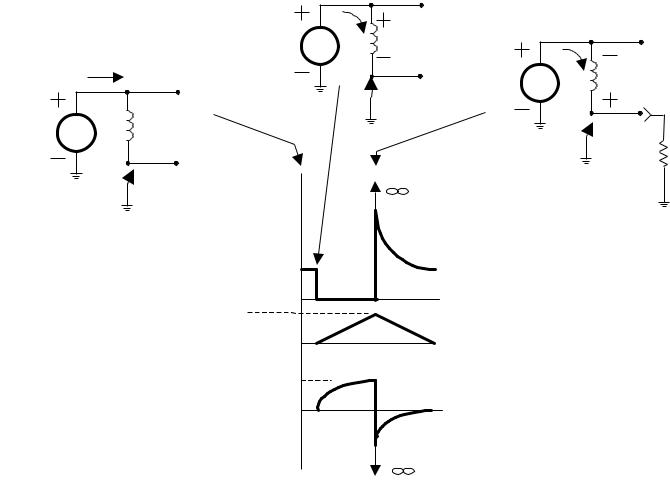
*dt* ∆*t*

or L times the change in current per unit time, the voltage approaches negative infinity (the inductor reverses polarity). Because the inductor is not ideal, it contains some amount of series resistance, which loads this “infinite” voltage to a finite number. With the switch open, and the inductor dis-charging, the voltage across it reverses and becomes additive with the source voltage VIN. If a diode and capacitor were connected to the output of this circuit, the capacitor would charge to this high voltage (perhaps after many switch cycles). This is how boost converters boost voltage, as shown in Figure 8.

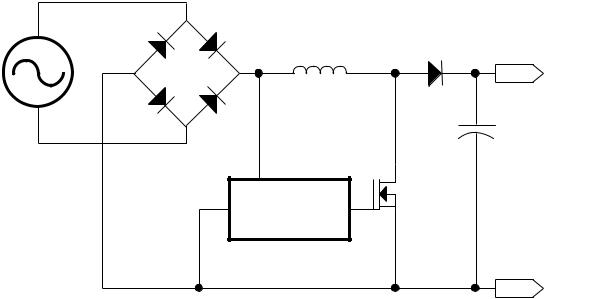
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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| IL | | Vi | |  | |  |
| L | VL | |  | | Vi |  |
|  | |  |  |
| Vin |  | |  | |  |  |
|  | Vo | |  | |  |  |
|  |  | | Vin | |  |  |
|  | Imax | | 0 | | Vo |  |
|  |  | |  |  |
|  |  | | 0 | | IL |  |
|  |  | | Vin | | VL |  |
|  |  | | 0 | |  |



**Figure 7. Flyback Action of an Inductor**



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | D1 |  |  |  |
| V1 – | + | Lp | D2 |  |
| Vo |  |
|  |  |  |  |
|  | Iin |  | Cin |  |
|  |  |  |  |
|  |  | PWM | Q1 |  |
|  | CONTROL | |  |  |
|  |  |  | RTN |  |

**Figure 8. PFC Boost Pre-Regulator**

The input to the converter is the full-rectified AC line volt-age. No bulk filtering is applied following the bridge recti-fier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. The boost converter must meet two simultaneous conditions: 1) the output voltage of the boost converter must be set higher than the peak value (hence the word boost) of the line voltage (a commonly used value is 385VDC to allow for a high line of 270VACrms), and 2) the current drawn from the line at any given instant must be proportional to the line voltage.

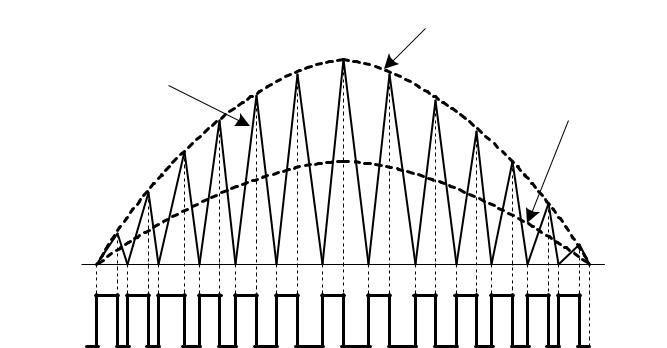
Without using power factor correction a typical switched-mode power supply would have a power factor of around

0.6, therefore having considerable odd-order harmonic dis-tortion (sometimes with the third harmonic as large as the fundamental). Having a power factor of less than 1 along with harmonics from peaky loads reduces the real power available to run the device. In order to operate a device with these inefficiencies, the power company must supply addi-tional power to make up for the loss. This increase in power causes the power companies to use heavier supply lines, oth-erwise self-heating can cause burnout in the neutral line con-ductor. The harmonic distortion can cause an increase in operating temperature of the generation facility, which reduces the life of equipment including rotating machines, cables, transformers, capacitors, fuses, switching contacts, and surge suppressors. Problems are caused by the harmon-ics creating additional losses and dielectric stresses in capacitors and cables, increasing currents in windings of

rotating machinery and transformers and noise emissions in many products, and bringing about early failure of fuses and other safety components. They also can cause skin effect, which creates problems in cables, transformers, and rotating machinery. This is why power companies are concerned with the growth of SMPS, electronic voltage regulators, and converters that will cause THD levels to increase to unacceptable levels. Having the boost preconverter voltage higher than the input voltage forces the load to draw current in phase with the ac main line voltage that, in turn, rids harmonic emissions.

**Modes of Operation**

There are two modes of PFC operation; discontinuous and continuous mode. Discontinuous mode is when the boost converter’s MOSFET is turned on when the inductor current reaches zero, and turned off when the inductor current meets the desired input reference voltage as shown in Figure 9. In this way, the input current waveform follows that of the input voltage, therefore attaining a power factor of close to 1.



|  |  |  |
| --- | --- | --- |
|  | Inductor Peak Current |  |
| Inductor |  |  |
| Current | Inductor Average |  |
|  |  |
|  | Current |  |

Gating

Signal

**Figure 9. Discontinuous mode of operation**

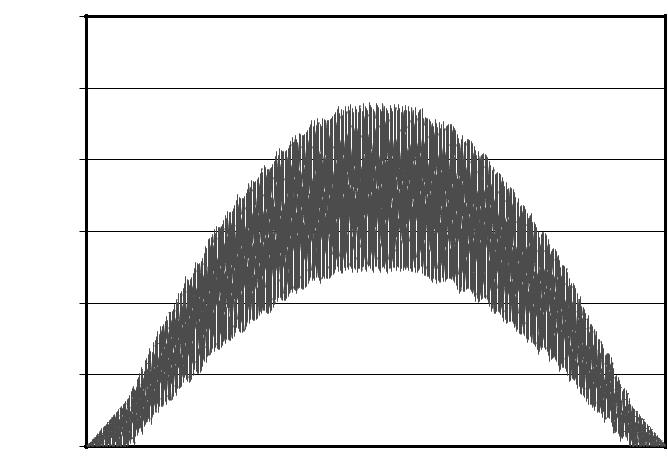
Discontinuous mode can be used for SMPS that have power levels of 300W or less. In comparison with continuous mode devices, discontinuous ones use larger cores and have higher I2R and skin effect losses due to the larger inductor current swings. With the increased swing a larger input filter is also required. On the positive side, since discontinuous mode devices switch the boost MOSFET on when the inductor cur-rent is at zero, there is no reverse recovery current (IRR) specification required on the boost diode. This means that less expensive diodes can be used.

Continuous mode typically suits SMPS power levels greater than 300W. This is where the boost converter’s MOSFET does not switch on when the boost inductor is at zero current, instead the current in the energy transfer inductor never reaches zero during the switching cycle (Figure 10).

With this in mind, the voltage swing is less than in discontin-uous mode—resulting in lower I2R losses—and the lower ripple current results in lower inductor core losses. Less voltage swing also reduces EMI and allows for a smaller input filter to be used. Since the MOSFET is not being turned on when the boost inductor’s current is at zero, a very fast reverse recovery diode is required to keep losses to a minimum.

|  |  |
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|  |  |  |  |
| --- | --- | --- | --- |
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|  | 3 | **Continuous Mode:** |  |
|  | *Average Current Mode* |  |
|  |  |  |
| **(A)** | 2.5 | The heart of the PFC controller is the gain modulator. The |  |
|  |  |
| **Current** | 2 | gain modulator has two inputs and one output. As shown in |  |
|  |  |
|  | Figure 13, the left input to the gain modulator block is called |  |
|  |  |  |
| **(Line)** | 1.5 | the reference current (ISINE). The reference current is the |  |
| input current that is proportional to the input full-wave-recti- |  |
|  |  |
|  |  |  |
| **Inductor** | 1 | fied voltage. The other input, located at the bottom of the |  |
| gain modulator, is from the voltage error amplifier. The error |  |
|  |  |
|  |  | amplifier takes in the output voltage (using a voltage divider) |  |
|  | 0.5 | after the boost diode and compares it to a reference voltage |  |
|  |  | of 5 volts. The error amplifier will have a small bandwidth so |  |
|  | 0 | as not to let any abrupt changes in the output or ripple errati- |  |
|  | **Figure 10. Continuous Mode of Operation** | cally affect the output of the error amplifier. |  |
|  |  |  |

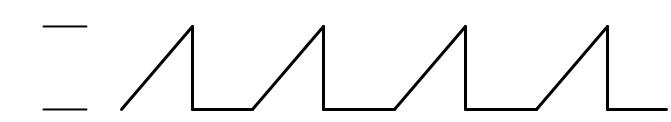


Fairchild offers products for all discontinuous and continu-ous modes of PFC operation, including critical conduction mode (FAN7527B), average current mode (FAN4810), and input current shaping mode (FAN4803).

**Discontinuous Mode:**

*Critical Conduction Mode*

A Critical Conduction mode device is a voltage mode device that works in the area between continuous and dis-continuous mode. To better explain critical conduction mode lets look at the difference between discontinuous and contin-uous mode in a SMPS design such as a flyback converter. In discontinuous mode, the primary winding of the transformer has a dead time once the switch is turned off (including is a minimum winding reset time) and before it is energized again (Figure 11).

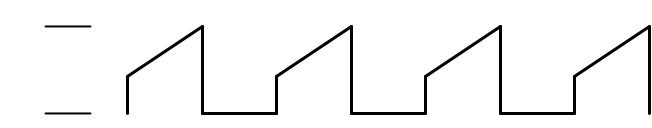


Ipk

0

**Figure 11. Discontinuous Mode, Flyback Power Supply Ip (Primary Current)**

In continuous mode, the primary winding has not fully depleted all of its energy. Figure 12 shows that the primary winding does not start energizing at zero, rather residual current still resides in the winding.



Ipk

0

**Figure 12. Continuous Mode, Flyback Power Supply IP (Primary Current)**

In critical conduction mode there are no dead-time gaps between cycles and the inductor current is always at zero before the switch is turned on. In Figure 9, the ac line current is shown as a continuous waveform where the peak switch current is twice the average input current. In this mode, the operation frequency varies with constant on time.

The gain modulator multiplies or is the product of the refer-ence current and the error voltage from the error amplifier (defined by the output voltage).

Figure 13 shows the critical blocks within the ML4821

(a stand alone PFC controller) to produce a power factor of greater than 95 percent. These critical blocks include the cur-rent control loop, voltage control loop, PWM control, and the gain modulator.

The purpose of the current control loop is to force the current waveform to follow the shape of the voltage waveform. In order for the current to follow the voltage, the internal cur-rent amplifier has to be designed with enough bandwidth1 to capture enough of the harmonics of the output voltage. This bandwidth is designed using external capacitors and resis-tors. Once the bandwidth has been designed which in most cases is a few kHz (to not be affected by any abrupt tran-sient), it uses information from the gain modulator to adjust the PWM control that controls whether the power MOSFET is switched on or off.

The gain modulator and the voltage control loop2 work together to sample the input current and output voltage,3 respectively. These two measurements are taken and than compared against each other to determine if a gain should be applied to the input of the current control. This decision is than compared against a sample of the output current to determine the duty cycle of the PWM.

The PWM control uses trailing-edge modulation as shown in Figure 14.

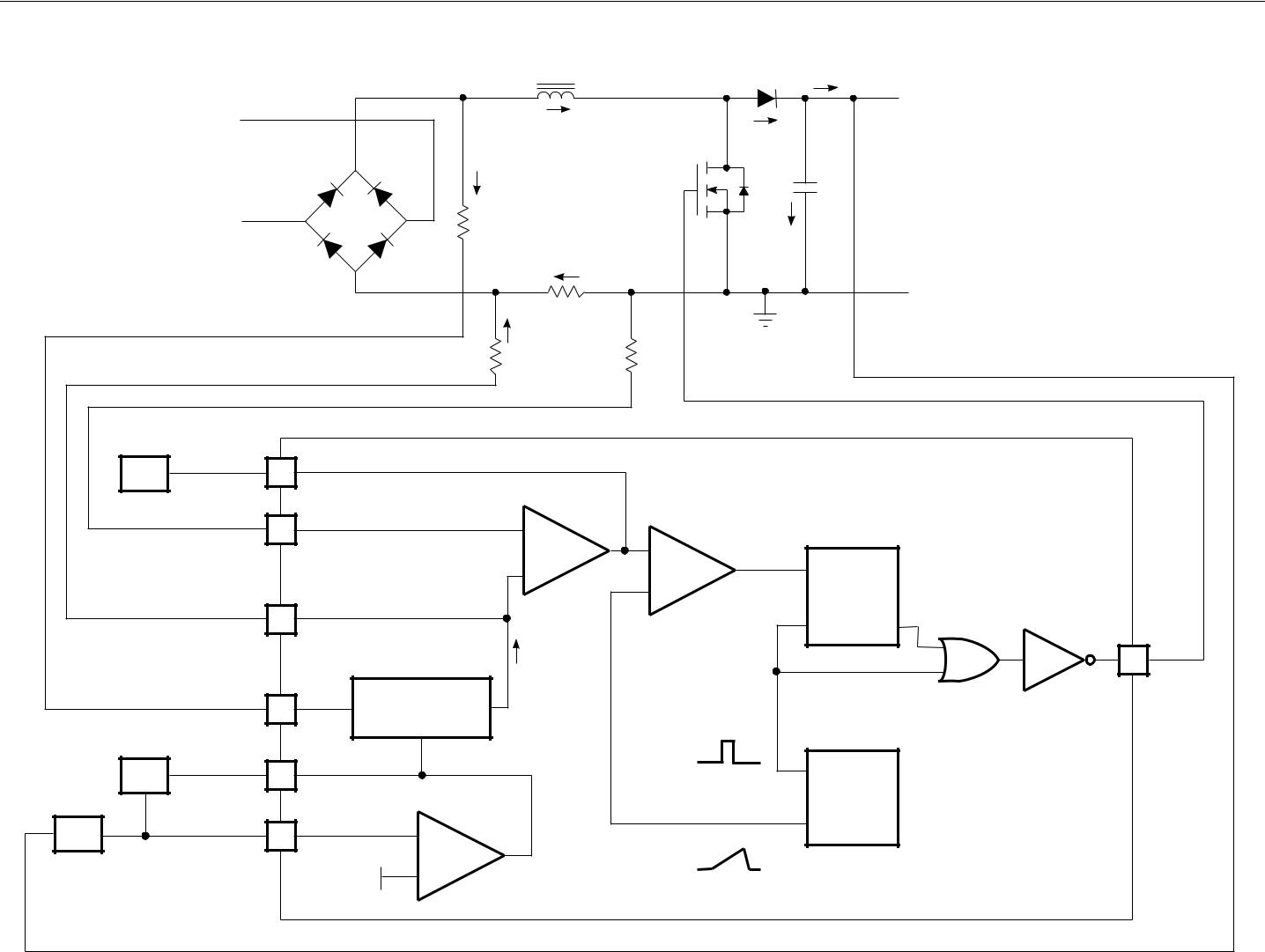
1The bandwidth is set by Fswitching/6

2The voltage control loop also needs to be bandwidth limited, Again, this is designed using external passive components.

3The output voltage of a continuous inductor current boost regulator has to be set above the maximum peak of the input voltage in order to function correctly as a PFC. The output should be 1.414 times the maximum input voltage.

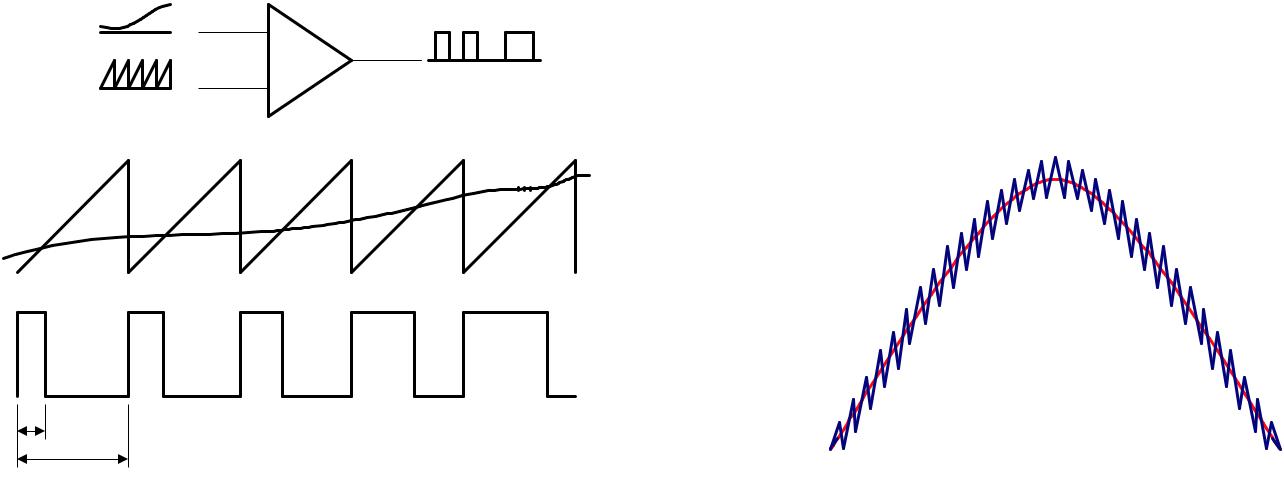
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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **APPLICATION NOTE** |  |  |  |  | **AN-42047** |  |
|  | DC IN | I |  | D | ILOAD |  |
|  |  |  |  |  |  |
|  |  | IL |  |  | + |  |
|  |  | Q | ID |  |  |
|  |  |  |  |  |
| AC | + |  |  |  |  |
|  |  | C | DC |  |
| IN |  | IPR |  |  |
|  |  |  |  |
|  | DBR | RL |  | IC | OUT |  |
|  |  |  |  |  |
|  | – | IL |  |  | – |  |
|  |  |  |  |  |
|  |  | RS |  |  |  |  |
|  |  | IGM |  |  | Voltage Control Loop |  |
| Current Control Loop |  | RC | RCL |  |  |
|  |  |  |  |



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| IA OUT | 2 |  |  |  |  |  |
| ZCF |  |  |  |  |  |
| IA– | 3 |  | – |  |  |  |
|  |  | – |  |  |
|  |  |  |  |  |  |
|  |  |  | + | R |  |  |
| IA+ |  |  |  | + |  |  |
| 4 |  |  | S |  |  |
|  |  |  | Q |  |
|  |  |  |  |  |
|  |  |  |  |  | OUT |  |
|  |  |  | IGM |  | 14 |  |
| ISINE | 5 |  | GAIN |  |  |  |
|  | MODULATOR | |  |  |  |
|  |  |  |  |  |
| EA OUT |  |  |  | Clock |  |  |
|  |  |  |  |  |  |
| ZF | 6 |  |  |  |  |  |
|  |  |  |  |  | OSC |  |
| INV | 7 |  | – |  |  |  |
| ZI |  | Ramp |  |  |
|  |  |  | E/A |  |  |
|  |  | VREF |  |  |  |
|  |  | + |  |  |  |

**Figure 13. Example of an Average Current Mode PFC Control (ML4821)**



+

–

Current

Reference

Input

Inductor Current

TON Output

TS

**Figure 14. Trailing-Edge Modulation4** **Figure 15. Typical Average Current Mode Waveform**

1. Trailing edge modulation is when the output switches on when the output of the comparator passes through the trailing edge of the sawtooth wave created.

|  |  |
| --- | --- |
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The line that goes through the saw tooth waveform is the out-put of the differential amplifier within the current loop con-trol. The output of the differential amplifier (located on the top of Figure 13) goes into an R-S flip flop that controls the power MOSFET. The average current mode waveform is shown in Figure 14. Figure 15 shows the waveform of what a typical average current PFC device looks like.

**Continuous Mode:**

*Input Current Shaping*

Using the continuous mode characteristic, the following equations show that the inductor current is proportional to the sinusoidal waveform at the turn-on time. Therefore the inductor current minimum value during one switching cycle follows the sinusoidal current reference as shown in Figure

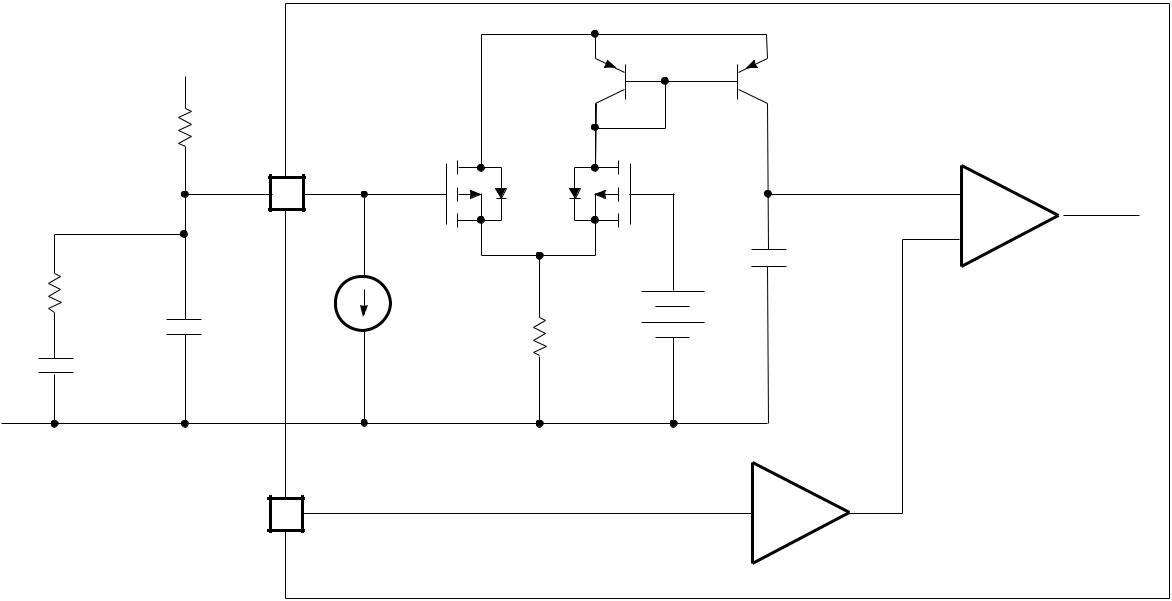
1. However, the inductor current peak value during one switching cycle is not controlled to follow the sinusoidal ref-erence. Therefore the average inductor current might not be sinusoidal. To make the average inductor current close to the sinusoidal reference, the inductance has to be high enough to make the current ripple small.

Fairchild’s FAN4803 features input current shaping, another control method of the continuous current mode PFC. Figure 16 shows the internal PFC block of the FAN4803. Unlike the conventional/typical average current mode PFC controller, the FAN4803 does not need input voltage information and a multiplier. It changes the slope of an internal ramp according to the error amplifier output voltage, while the current sense information and the ramp signal are used to determine the turn-on time. As shown in Figure 17a, the switch is turned on when the current sense voltage meets the internal ramp sig-nal and the switch is turned off by the internal clock signal. To control the output voltage, the slope of the internal ramp signal is adjusted. By comparing Figure 17a and Figure 17b, one can see that the average current increases if the slope increases and decreases if the slope decreases.

VOUT = 400V

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| *VL* | = *VIN* | = *L* | *diL* | |  | | | | | | | | |  | |  | |  | |  | |  | |  | |  | | |  |  |
| *ton* | | | | | | | | | | |  | |  | |  | |  | |  | |  | |  | | |  |  |
|  |  |  |  | |  | |  | |  | |  | |  | |  | | |  |  |
| *VL* | = (*VIN* | − *VOUT* ) = *L* | | | | | | | | *diL* | | | | | | | |  | |  | |  | |  | |  | | |  |  |
| *toff* | | | |  | |  | |  | |  | |  | |  | |  | | |  |  |
|  |  |  |  | |  |  | |  | |  | |  | |  | |  | |  | |  | |  | | |  |  |
| *VIN* • *ton* =(*VOUT* − *VIN* )• *toff* , | | | | | | | | | | | | | | | | | | | *toff* | | | | = | | | | *VIN* | | |  |
| *T* | | *S* | | *V* | | |  |
|  |  |  | |  |  | |  | |  | |  |  |  | |  | |  | |  | |  | |  | | *OUT* | | |  |
| *VCS* | = *Vramp* = *Veao* | | | | | | | | *toff* | | | |  | | = *Veao* | | | | | | | |  | | *VIN* | | |  | |  |
| *TS* | | | | | | *VOUT* | | | | | | |  |
|  |  |  | |  |  | |  | |  | |  | |  | |  | |  |
| *Rs* • *iL* (*tO* | | + *toff* ) = | | | | | *Veao* | | | | | *VIN* •sin(*ω t*) | | | | | | | | | | | | | | | | | |  |
|  | | | | |  |
|  |  |  |  | |  | *VOUT* | | | | | | | |  | |  | |  | |  | |  | |  | |  | | |  |  |

∴ *I L*(min)= *iL* (*tO* + *toff* )∝sin(*ω t*)



* + During on-time
* During off-time
* CCM condition
  + Switch off to on instant

RP

VEAO

VC1

Gate

4

–

Output

|  |  |  |  |
| --- | --- | --- | --- |
| RCOMP |  | 35µA |  |
|  | CCOMP |  |
|  | R1 |  |
|  |  |  |
| CZERO |  |  |  |

ISENSE

3

COMP

C1 +

30pF

5V

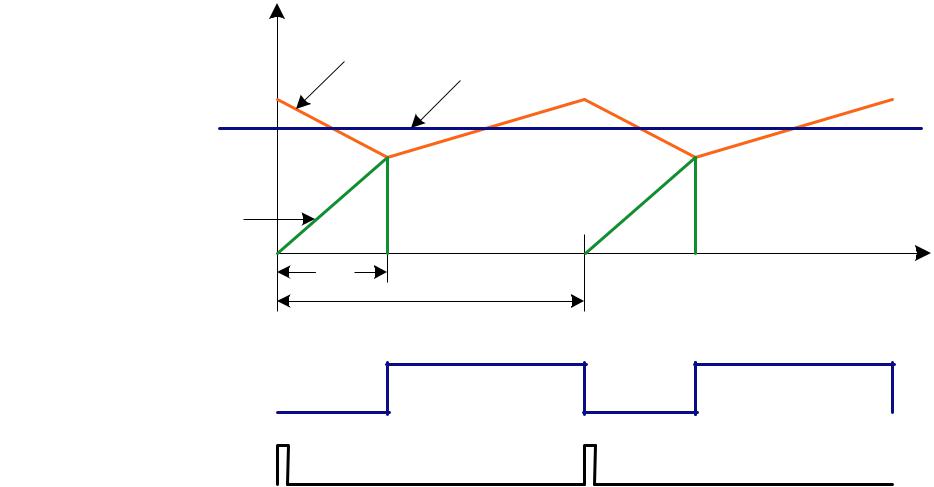
–4

VI SENSE

**Figure 16. Example of the Input Current Shaping PFC Controller (FAN4803**

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|  |  |
| --- | --- |
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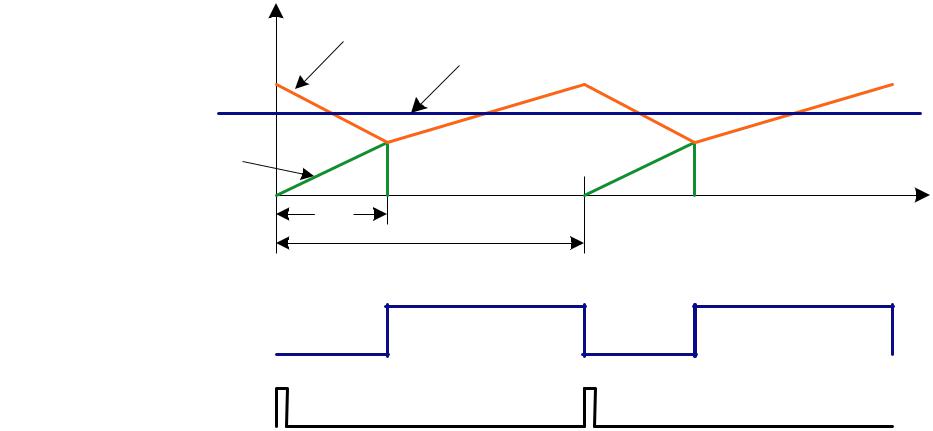
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Vramp = Veao (toff / TS) |  | Vcs |  | Average Current | |  |
| Vcs = Rs • iL |  |  |  |  |
|  |  |  |  |  |  |
| Vramp |  |  |  |  |  |  |
| to | t | off | to | + toff | to +T |  |
|  |  |  |  | S |  |
|  |  |  |  | TS |  |  |

PFC OUT

Clock

**Figure 17a. Typical Input Current Shaping PFC Waveform**

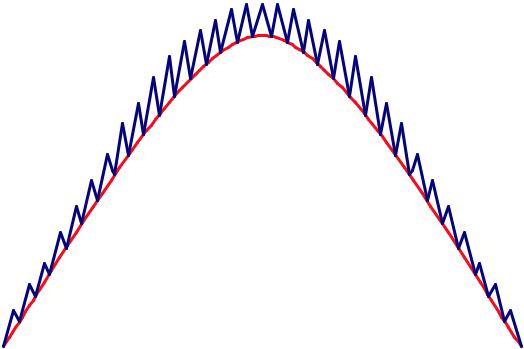
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Vramp = Veao (toff / TS) |  | Vcs | Average Current | | | |  |
| Vcs = Rs • iL |  |  |  |
|  |  |  |  |  |  |  |
| Vramp |  |  |  |  |  |  |  |
| to | toff | to | + toff | t | o | +T |  |
|  |  |  |  |  | S |  |
|  |  |  | TS |  |  |  |  |



PFC OUT

Clock

**Figure 17b. Typical Input Current Shaping PFC Waveform**



Inductor

Current

Current

Reference

**Figure 18. Input Current Shaping PFC Waveform**

|  |  |
| --- | --- |
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**AN-42047** **APPLICATION NOTE**

**Leading Edge Modulation/Trailing Edge Modulation (LEM/TEM) versus Trailing Edge Modulation/Trailing Edge Modulation (TEM/TEM)**

Leading edge/trailing edge modulation is a patented Fair-child technique to synchronize the PFC controller to the PWM controller. Typically TEM/TEM is used in PFC/PWM controllers which results in an additional step as well as a larger PFC bulk capacitor (as shown below).

**Trailing Edge Modulation/Trailing Edge Modulation (TEM/TEM)**

Figure 19a shows the PFC inductor being energized.

Figure 19b shows the energy from the inductor being trans-ferred into the PFC bulk capacitor.

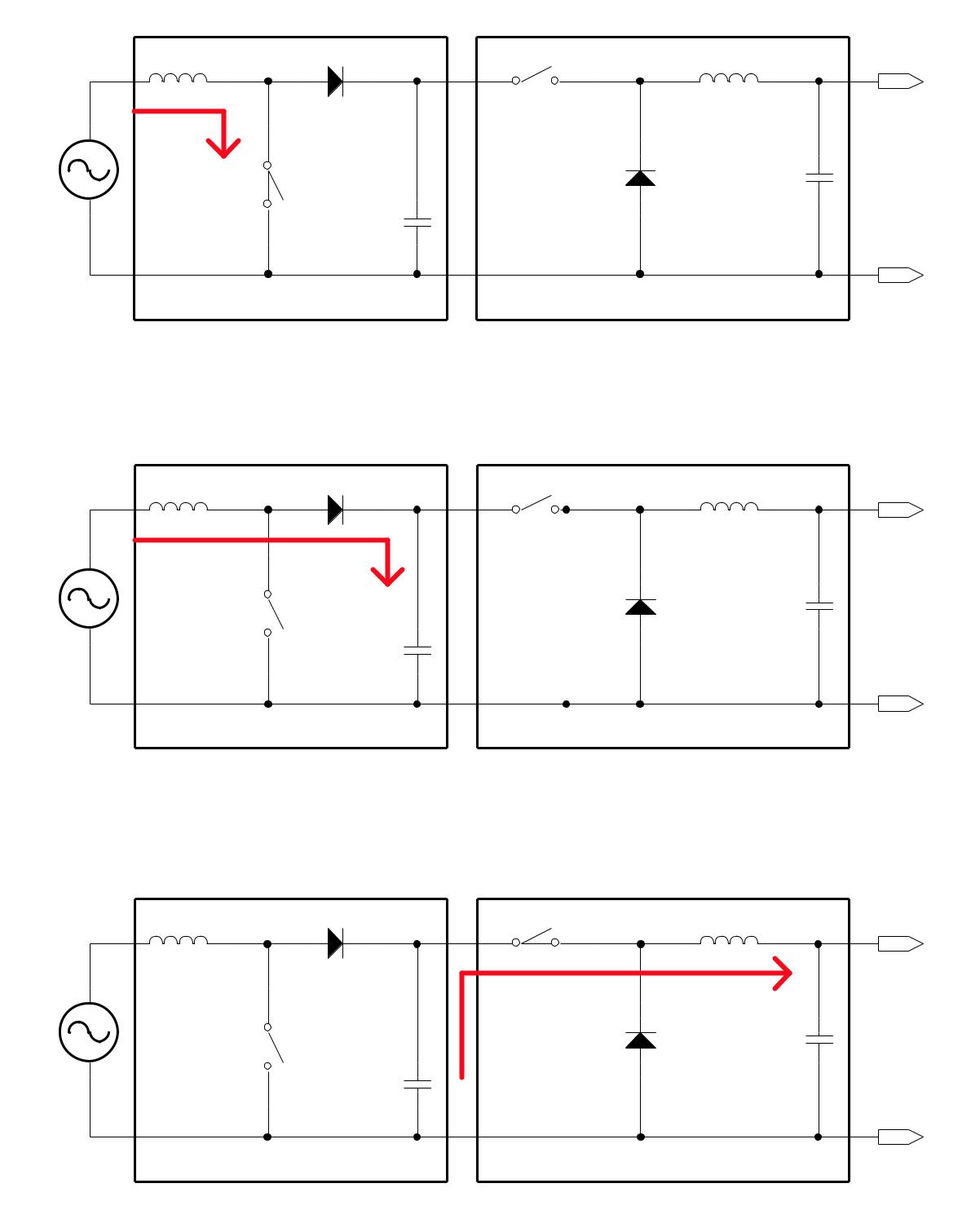
When the PWM switch is closed, as shown in Figure 19c, the energy stored within the PFC bulk capacitor is used to drive the load. Every time this cycle is repeated, the PFC bulk capacitor has to be fully charged since it is fully discharged when the PWM switch is closed.

**Fairchild Patented Leading Edge Modulation/ Trailing Edge Modulation (LEM/TEM) Technique**

In LET/TEM the PFC and PWM switches are tied together, but opening and closing 180 degrees out of phase, so when the PFC switch is open the PWM switch is closed and vice versa. Initially when the PFC switch is closed, the PFC inductor is energized, once the PWM switch is closed, both the output and the PFC bulk capacitor are energized. Figures 20a and 20b show that upon repetition of this cycle, the PFC bulk capacitor does not have to be that large because it is not powering the output all by itself, the PFC inductor is helping out as well.

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|  |  |
| --- | --- |
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|  |  |



Signal

AC

Signal

AC

Signal

AC

**PFC Section** **PWM Section**

Open

Vout

Current

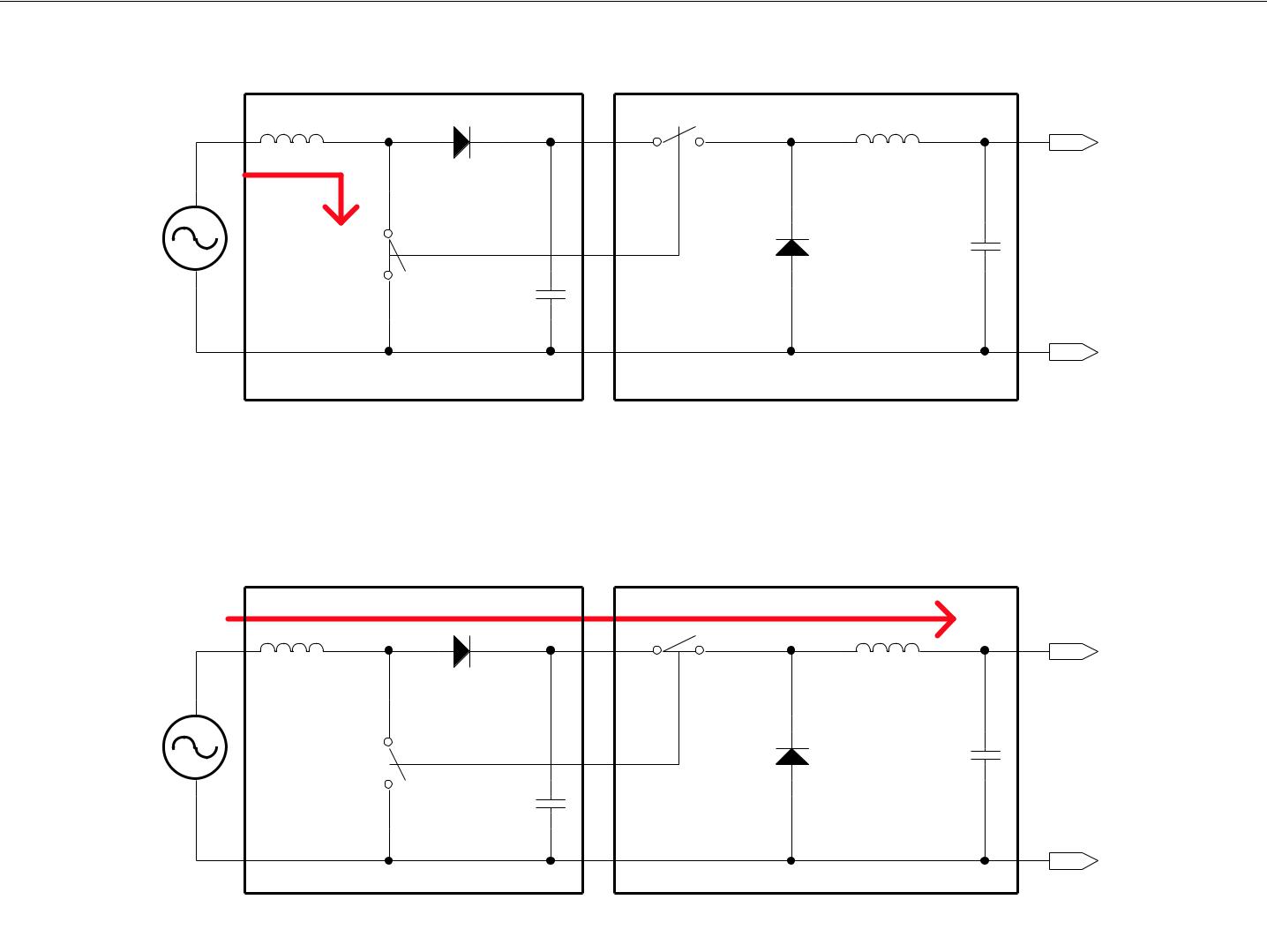
|  |  |  |
| --- | --- | --- |
|  | Output |  |
| Closed | Cap |  |
| PFC Bulk |  |  |
| Cap |  |  |
|  | GND |  |
| **Figure 19a. Energizing the PFC Inductor** | |  |
| **PFC Section** | **PWM Section** |  |
|  | Open |  |
|  | Vout |  |
| Current |  |  |
|  | Output |  |
| Open | Cap |  |
|  |  |
| PFC Bulk |  |  |
| Cap |  |  |
|  | GND |  |
| **Figure 19b. Charging the PFC Bulk Capacitor** | |  |
| **PFC Section** | **PWM Section** |  |
|  | Closed |  |
|  | Vout |  |
|  | Current |  |
|  | Output |  |
| Open | Cap |  |
| PFC Bulk |  |  |
| Cap |  |  |

GND

**Figure 19c. Powering the Output**

|  |  |
| --- | --- |
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**AN-42047** **APPLICATION NOTE**



|  |  |  |  |
| --- | --- | --- | --- |
|  | **PFC Section** | **PWM Section** |  |
|  |  | Open |  |
|  |  | Vout |  |
| Signal | Current |  |  |
|  | Output |  |
| AC |  |  |
|  | Closed | Cap |  |
|  |  |  |
|  | PFC Bulk |  |  |
|  | Cap |  |  |
|  |  | GND |  |

**Figure 20a. Energizing the PFC Inductor**

|  |  |  |
| --- | --- | --- |
| **PFC Section** | **PWM Section** |  |
|  | Current |  |
|  | Vout |  |
| Signal | Closed |  |
|  |  |
| AC | Output |  |
|  |  |
| Open | Cap |  |
|  |  |
| PFC Bulk |  |  |
| Cap |  |  |
|  | GND |  |

**Figure 20b. Charging the PFC Bulk Capacitor and Powering the Output**

**Conclusion**

Power companies do not get excited over low power factor

driven devices, plus the extra cost of unused or wasted power

can be quite large. This is why PFC on the device side has

become an important part of the final power system design

for so many products. There are many standards in place

(example, EN 61000-3-2) to drive power consumption to a

power factor of 1 and keep total harmonic distortion to a

minimum. Depending on the output power and the designer’s

needs, a SMPS can be designed with either a discontinuous

or continuous mode stand alone PFC controller, or a continu-

ous PFC/PWM mode device can be used. PFC controllers

are forecasted to grow to $175 million in 2006, and stan-

dards are reducing the minimum power limits on systems

that require PFC, more and more PFC controllers will be

used.

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**AN-42047** **APPLICATION NOTE**

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